

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (previously presented) A method for forming contact plugs on active regions of a semiconductor device, the method comprising:
  - forming a plurality of gate lines on a substrate;
  - implanting first dopants of first conductivity type into the substrate using the gate lines as a mask to form a plurality of cell junctions, each gate line being provided between two cell junctions;
  - forming a buffer layer over the cell junctions; and
  - implanting second dopants of first conductivity type through the buffer layer and into the cells junctions using a first energy level to form a plurality of plug ion-implantation regions, the plug ion-implantation regions being configured to receive the contact plugs;
  - implanting the second dopants of first conductivity type through the buffer layer and into the cell junctions using a second energy level that is different from the first energy level to form the plug ion-implantation regions; and
  - forming a well of second conductivity type within the substrate, wherein the cell junctions and the plug ion-implantation regions are defined within the well,
  - wherein the buffer layer is configured to enable a higher implantation energy to be used to implant the second dopants, so that a concentration profile of the second dopants has a reduced slope.
2. (previously presented) The method as recited in claim 1, wherein the second dopants are implanted to form the plug ion-implantation region by employing a blanket ion-implantation technique without using a mask, wherein the plug ion-implantation regions are formed by implanting the second dopants using at least two different energy levels, so that the concentration profile of the second dopants has a reduced slope to suppress a width of a

depletion layer from being decreased, the depletion layer being providing between the well and the cell junctions, wherein the well is formed before the cell junctions and plug ion-implantation regions.

3. (original) The method as recited in claim 2, wherein the blanket ion-implantation process proceeds by employing phosphorus  $^{31}\text{P}$  with a dose ranging from about  $1 \times 10^{12}$  ions/cm<sup>2</sup> to about  $3 \times 10^{13}$  ions/cm<sup>2</sup> and an implantation energy ranging from about 80 keV to about 150 keV.

4. (original) The method as recited in claim 2, wherein the blanket ion-implantation process proceeds by employing  $^{31}\text{P}$  with distributed energy within a range from about 80 keV to about 150 keV and dose within a range from about  $1 \times 10^{12}$  ions/cm<sup>2</sup> to about  $3 \times 10^{13}$  ions/cm<sup>2</sup> both being applied in several sets.

5. (original) The method as recited in claim 4, wherein the blanket ion-implantation process with distributed energy is carried out in several sets by increasing energy from a high level to a low level but within a range from about 80 keV to about 150 keV.

6. (previously presented) The method as recited in claim 1, wherein the buffer layer is a nitride layer, wherein the plug ion-implantation regions are formed by implanting the second dopants using at least two different energy levels, so that a concentration profile of the second dopants has a reduced slope.

7. (previously presented) The method as recited in claim 6, wherein the nitride layer has a thickness in a range from about 200 Å to about 500 Å.

8. (original) The method as recited in claim 1, wherein the first dopant and the second dopant are N-type dopants.

9. (previously presented) The method as recited in claim 1, further comprising:

- forming a spacer at both sidewalls of each gate line by etching the buffer layer;
- forming an inter-layer insulation layer on a resultant substrate structure;
- forming a plurality of contact holes exposing a surface of each cell junction by etching the inter-layer insulation layer; and
- forming a plurality of contact plugs electrically coupled to the cell junctions through the contact holes.

10-18. (canceled)

19. (previously presented) A method for forming contact plugs on a semiconductor device, the method comprising:

- forming a well of second conductivity type within a substrate;
- forming a plurality of gate structures on the substrate, the gate structures defining a plurality of regions;
- implanting first dopants of first conductivity type into the regions defined by the gate structures using the gate structures as a mask to form a plurality of cell junctions, so that each gate structure is provided between two cell junctions;
- forming a buffer layer over the regions defined by the gate structures; and
- implanting second dopants of first conductivity type through the buffer layer and into the regions defined by the gate structures using a first energy level to form a plurality of plug ion-implantation regions, the plug ion-implantation regions being configured to receive the contact plugs,

wherein the cell junctions and the plug ion-implantation regions are defined within the well,

wherein the second dopants are implanted into the substrate via the buffer layer to obtain a concentration profile of the second dopants in the substrate that has a reduced slope, and

wherein the reduced slope of the concentration profile of the second dopants suppresses a width of a depletion layer from being decreased, the depletion layer being provided between the well and the cell junctions.

20. (previously presented) The method of claim 19, further comprising:  
implanting the second dopants of first conductivity type through the buffer layer and into the regions defined by the gate structures using a second energy level that is different from the first energy level to form the plug ion-implantation regions,

wherein the plug ion-implantation regions are formed using at least two different energy levels to provide the concentration profile of the second dopants in the substrate with a reduced slope.